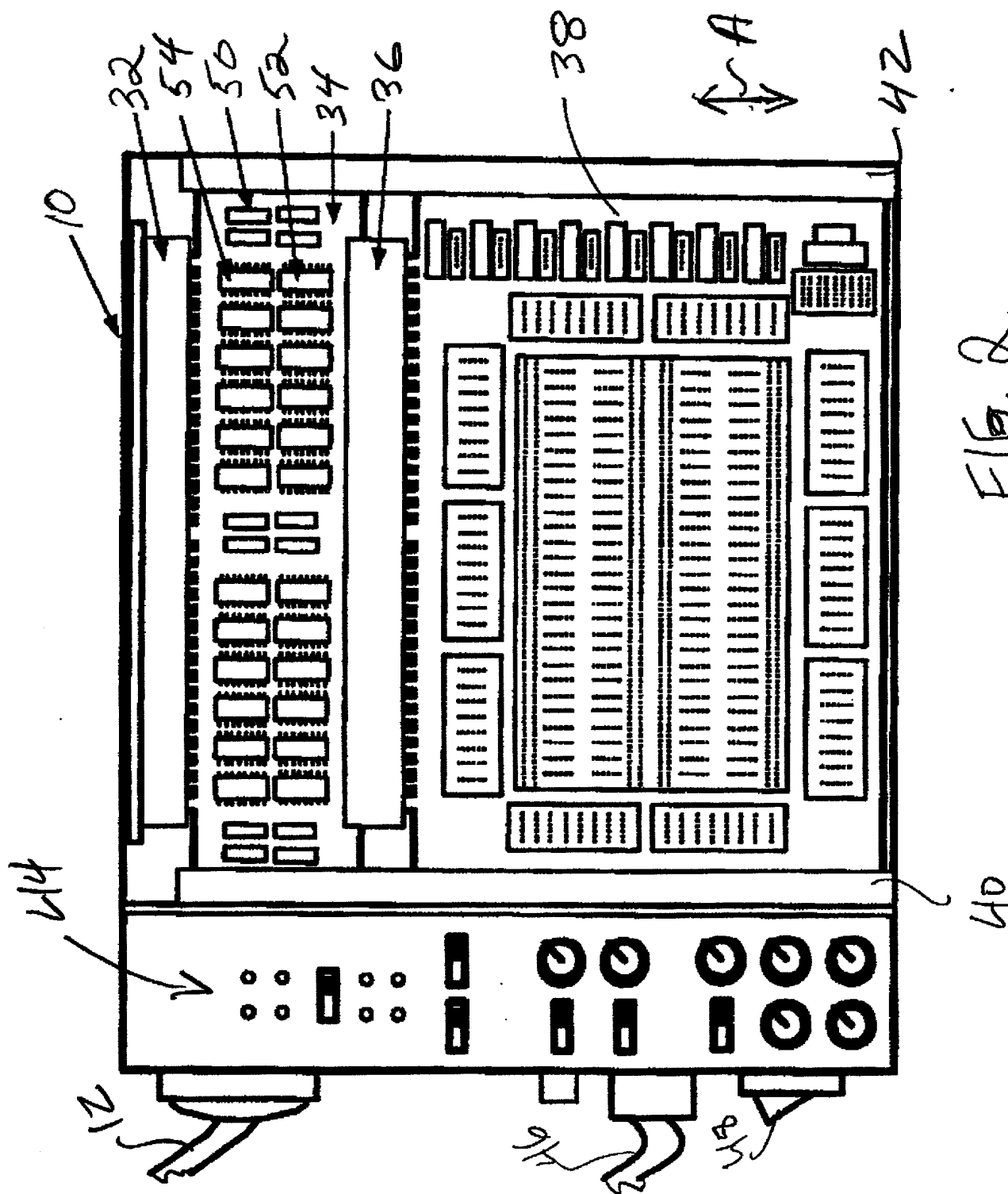


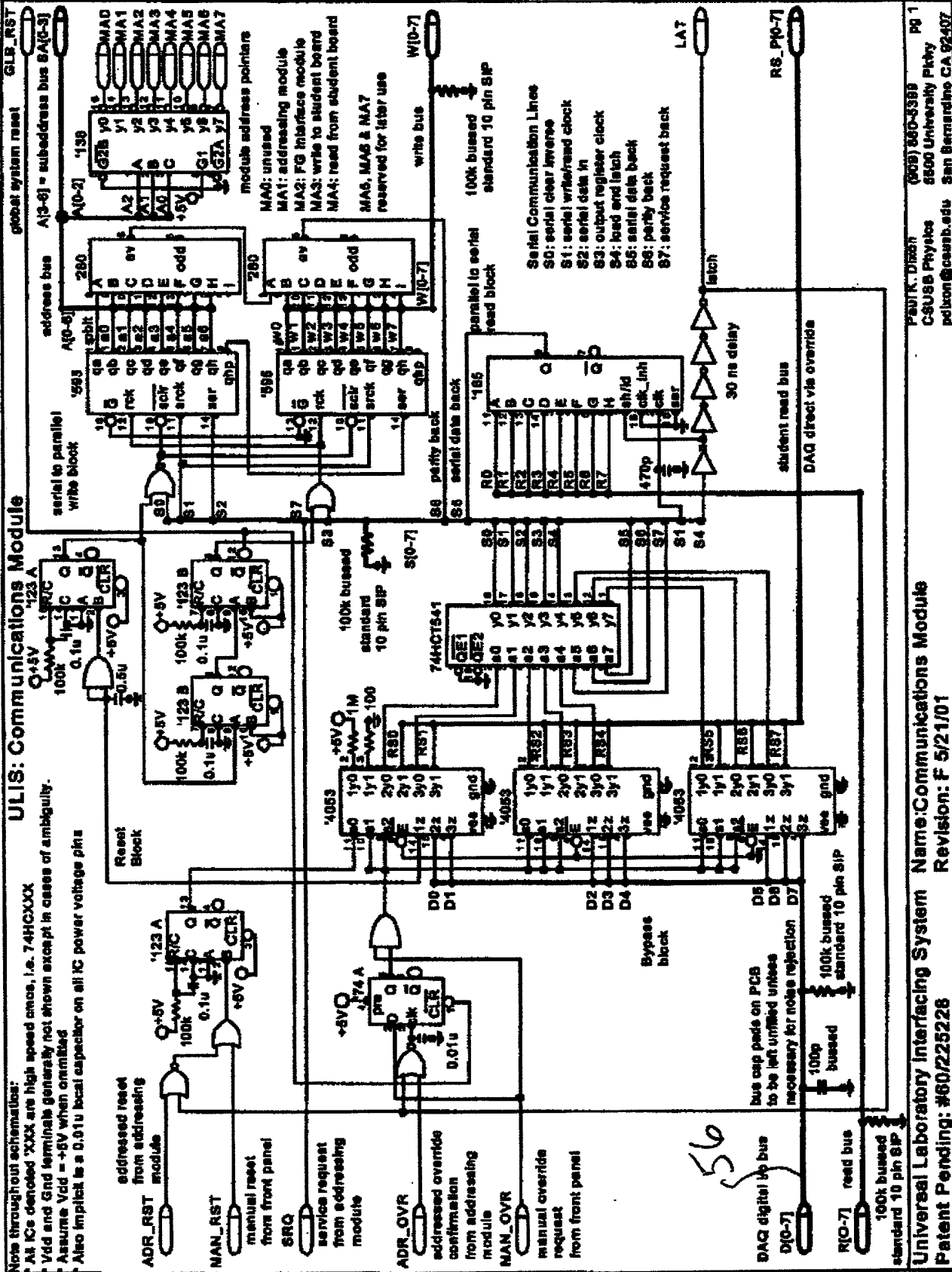
ULIS Block Diagram



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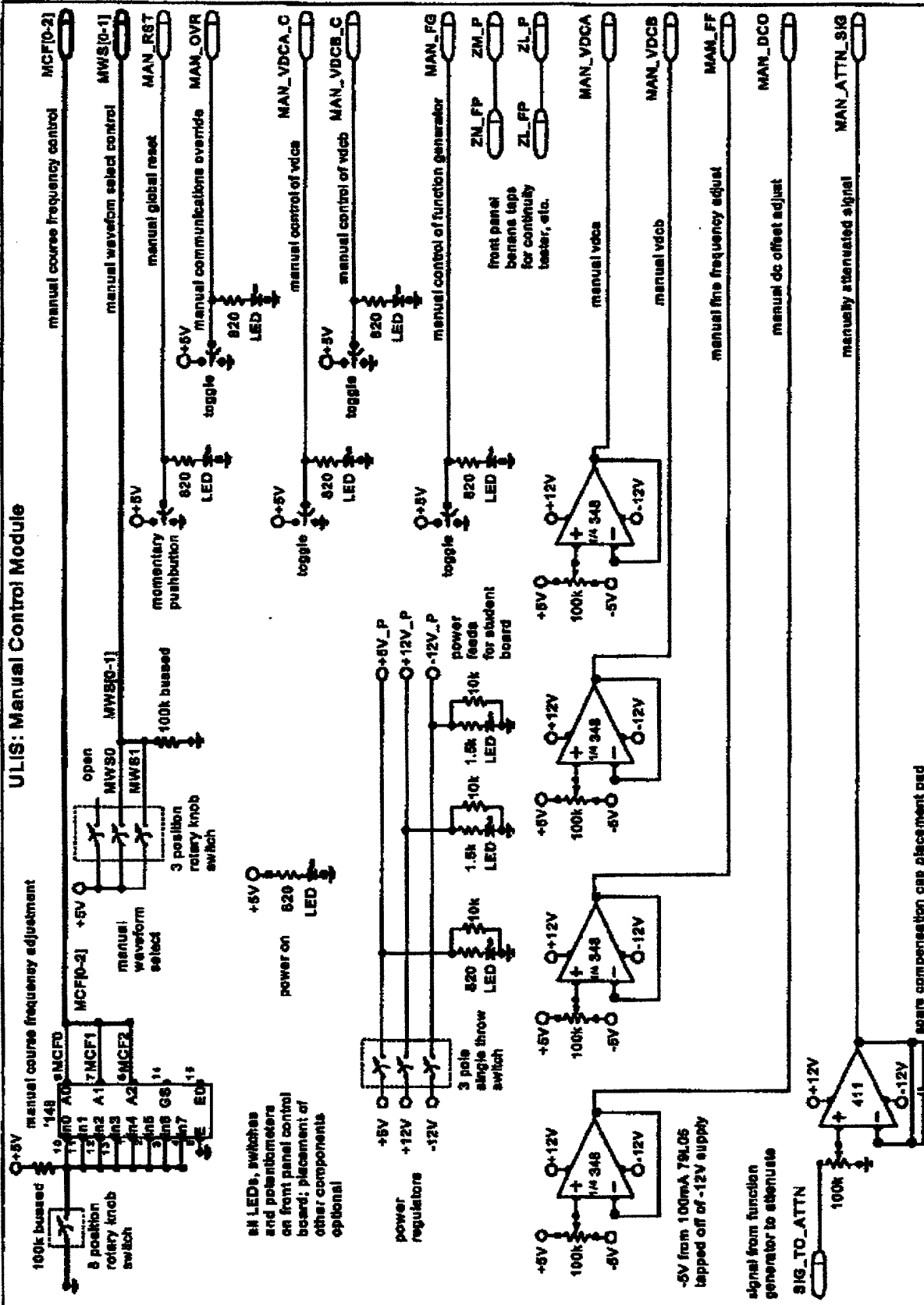
Dixon/Usher
Express Mail# ET 007354780
8/14/2001



F/G.3

Universal Laboratory Interfacing System Name: Communications Module
Revision: F 5/21/01
Patent Pending: #60225226
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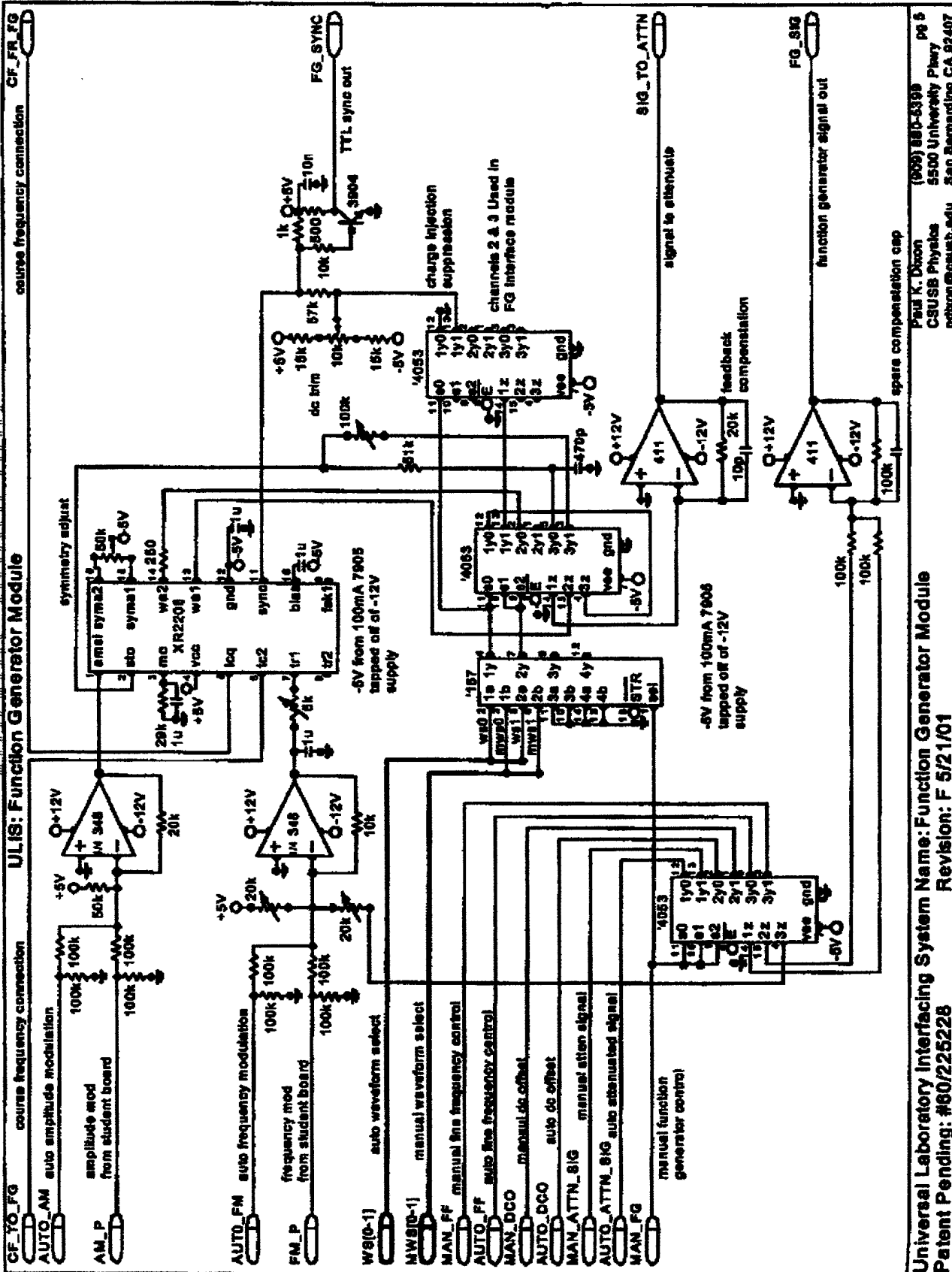
ULIS: Manual Control Module



Universal Laboratory Interfacing SystemName: Manual Control Module
Patent Pending: #60/225228 Revision: F 5/21/01

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Fig. 4



F16.5





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REC'D TO OE INF



power and ground connections

direct to earth ground GND ○ ——— ○ GND_SB student board ground plane

GND_DAQ_AI ○ ——— ○ GND_DAQ_AI_SB tie points across

+5V_P ○ ——— 1.5A fast ——— ○ +5V_SB

+12V_P ○ ——— 1.5A fast ——— ○ +12V_SB

-12V_P ○ ——— 1.5A fast ——— ○ -12V_SB

power connections on main board

power connections on student board side of protection board

analog out large signal connections

main board +12V_M ○ ——— 1.5A fast ——— ANALOG_LS_P ——— ANALOG_LS_SB

main board -12V_M ○ ——— 1.5A fast ———

signals: AOD, AO1, VDCA, VDCB, ZH, ZM, ZL

board presence connections

main +5V and ground +5V ○ ——— 100k ——— PS_PRES ——— PS_PRES_P ——— PS_PRES_SB

high on connection SB_PRES ——— 100k ——— SB_PRES_P ——— SB_PRES_SB

Internal protection board

these internal connections make no contact to student board power or ground

analog small signal connections

main board +12V_M ○ ——— 100 ——— ANALOG_SS_P ——— ANALOG_SS_SB

main board -12V_M ○ ——— 100 ———

signals: AIP-13, AISEN2E, PG_SIG, AM, FM

some direct to DAQ, others thru main circuit

voltmeter connections

+12V_M ○ ——— 500k ——— VOLT_METER_P ——— VOLT_METER_SB

-12V_M ○ ——— 500k ———

all diodes on main board

signals: VH, VL

digital connections

+5V_M ○ ——— 100 ——— DIGITAL_P ——— DIGITAL_SB

GND_M ○ ——— 100 ———

signals: SYNC_OUT, WSP-7, ASIP-6, RSIP-7, PFIP-6, CTR0_OUT, CTR1_OUT, SD_CLK, EXT_STR, FREQ_OUT

some direct to DAQ, others thru main circuit

General purpose analog/digital prototyping board has identifier:	
00000001	00000000
invalid	invalid
11111111	invalid

signals:	tree bit	head-wired connections	defining model number
SBIP-7	SBIP-7	SBIP-7	SBIP-7
SBIP-7	SBIP-7	SBIP-7	SBIP-7
SBIP-7	SBIP-7	SBIP-7	SBIP-7
SBIP-7	SBIP-7	SBIP-7	SBIP-7

all resistors in 16 pin DIP isolated packages, 300mW ceramic substrate (CTS 781-3-R100)

500 mA minimum current rating on all diodes

all diodes on main board

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Universal Laboratory Interfacing System Name: Protection Module

Revision: F 5/21/01

stent Pending: #80/225228

FIG. 9

Variable	Mean		SD		t		p	
	Control	Case	Control	Case	Control	Case	Control	Case
Age	20.5	20.5	1.5	1.5	0.0	0.0	0.999	0.999
Gender	100	100	0	0	0.0	0.0	0.999	0.999
Education	12.0	12.0	0.0	0.0	0.0	0.0	0.999	0.999
Occupation	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Marital status	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Religion	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Income	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Health status	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Family size	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental education	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental occupation	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental marital status	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental religion	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental income	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental health status	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental family size	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental education	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental occupation	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental marital status	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental religion	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental income	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental health status	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental family size	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental education	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental occupation	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental marital status	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental religion	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental income	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental health status	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental family size	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental parental education	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental parental occupation	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental parental marital status	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental parental religion	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental parental income	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental parental health status	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental parental family size	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental parental parental education	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental parental parental occupation	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental parental parental marital status	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental parental parental religion	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental parental parental income	1.0	1.0	0.0	0.0	0.0	0.0	0.999	0.999
Parental parental parental parental parental health status	1.0	1.0						

ULIS: Addressing, Digital I/O and Status Module

student address bus

module 1; addresses 16-31
18: unused & invalid
17: addressed override confirmation
16: addressed global reset
19: frequency measurement block
20: impedance analyzer block
21: analog i/o switching block
22: write test status byte
23: read current status byte
24: read serial number low byte
25: read model & version

student write bus
addresses: 40-53

WS_PD-7I

MA1

MA3 MA4 LAT GLB_RST MAN_OVR MAN_PG MAN_VDCA_C MAN_VDCB_C PB_PRES_P SB_PRES_P SV_F W(0-7) RS_PD-7I

SA10-3J

'A50 QAE1 QAE2
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

'A51 QAE1 QAE2
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

'A52 QAE1 QAE2
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

'A53 QAE1 QAE2
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

'A54 QAE1 QAE2
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

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'A167 QAE1 QAE2
Y0 Y1 Y2 Y3 Y4 Y5 Y6 Y7

'A168 QAE1 QAE2
Y0 Y1 Y2 Y

Fig. 10

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pg 2

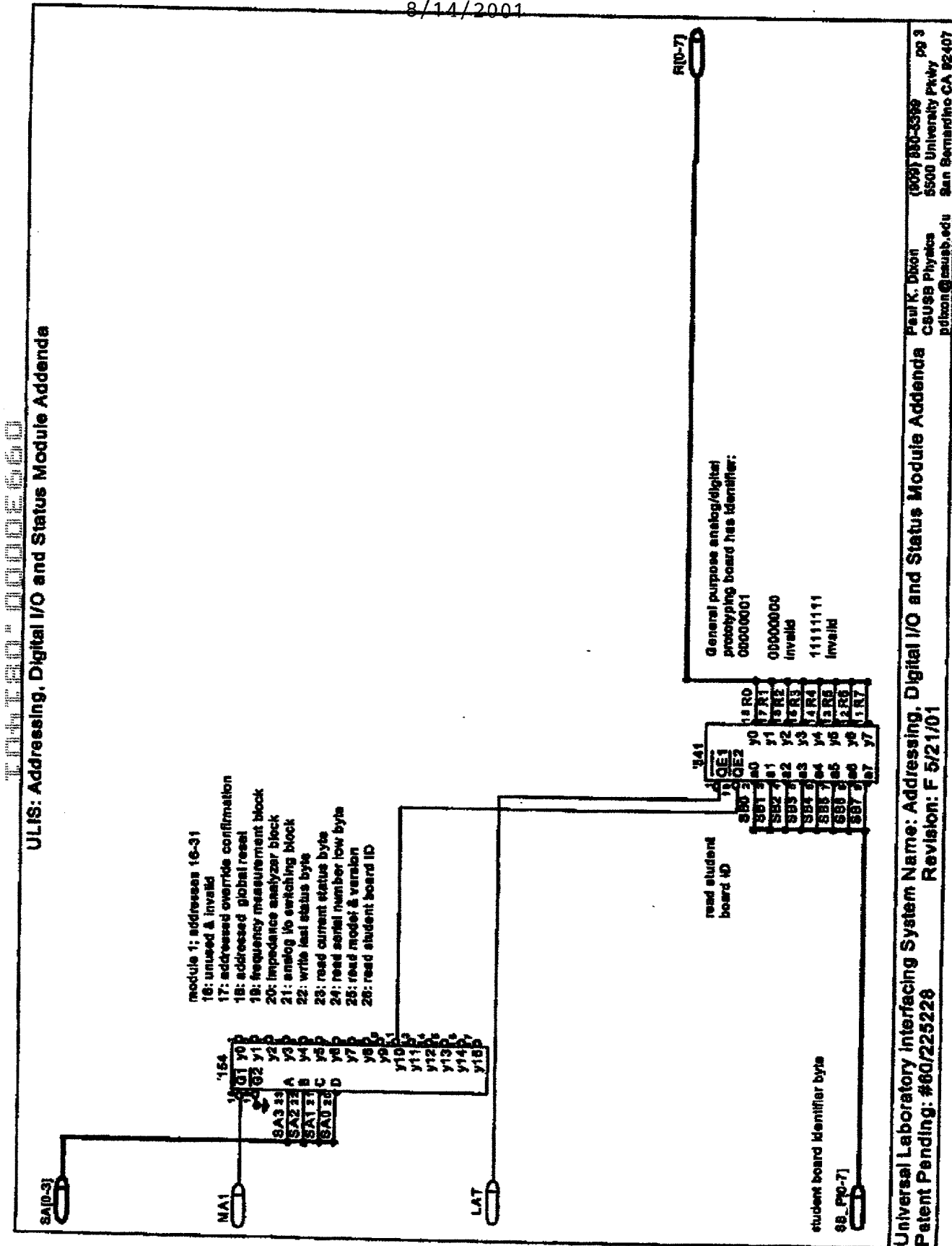
Name: Addressing, Digital I/O and Status Module
Revision: F 5/21/01

15-00000

Revision: F 5/21/01

Dixon/Usher
Express Mail # ET 007354780
8/14/2001

ULIS: Addressing, Digital I/O and Status Module Addenda



Universal Laboratory Interfacing System Name: Addressing, Digital I/O and Status Module Addenda
Patent Pending: #80/225228
Revision: F 5/21/01

F16.11